IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Patwardhan et al.

Attorney Docket No.: NSC1P131X3

Application No.: 10/707,208

Examiner: Not Yet Assigned

Filed: November 26, 2003

Group: Not Yet Assigned

Title: INTEGRATED CIRCUIT DEVICE PACKAGE HAVING A SUPPORT COATING FOR IMPROVED RELIABILITY DURING TEMPERATURE CYCLING

Confirmation No.: 1207

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on January 23, 2004 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____ Secretary

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

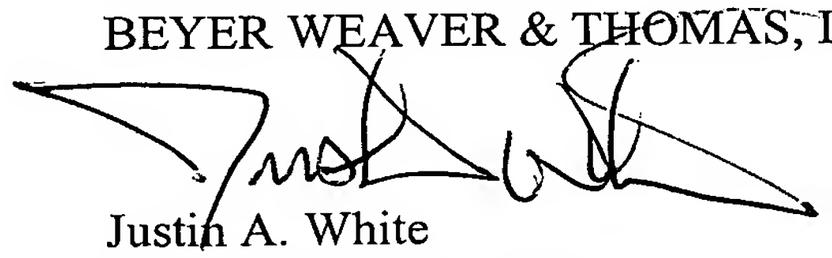
Dear Sir:

The references listed in the attached PTO Form 1449 may be material to examination of the above-identified patent application. Applicants submit the list of these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application. The above-identified application is a continuation-in-part of prior application U.S. Patent Application No. 10/224,291. This prior application is being relied upon for an earlier filing date under 35 U.S.C. § 120. Because the listed references (maked with an *) were either cited by the PTO, or submitted to the PTO in the prior application, under 37 CFR § 1.98(d) Applicants submit that copies need not be provided. Please note that references patents/articles (AA - DD), are enclosed since these references were not cited during the prosecution of the above-mentioned application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P131X3).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. NSC1P131X3 Applicant: Patwardhan et al. Filing Date 11/26/03	Application No.: 10/707,208 Group Not Yet Assigned

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
*	A	5,214,308	05/93	Nishiguchi et al.			
*	B	5,495,439	02/96	Morihara			
*	C	5,668,059	09/97	Christie et al.			
*	D	5,895,976	04/00	Morrell et al.			
*	E	5,872,633	02/99	Holzapfel et al.			
*	F	5,953,623	09/99	Boyko et al.			
*	G	6,060,373	05/00	Saitoh			
*	H	6,063,647	05/00	Chen et al.			
*	I	6,071,757	06/00	Fogal et al.			
*	J	6,121,689	09/00	Capote et al.			
*	K	6,130,473	10/00	Mostafazadeh et al.			
*	L	6,190,940	2/01	DeFelice et al.			
*	M	6,245,595	06/01	Nguyen et al.			
*	N	6,258,626	7/01	Wang et al.			
*	O	6,307,269	10/01	Akiyama et al.			
*	P	6,391,683	05/02	Chiu et al.			
*	Q	6,486,562	11/02	Kato			
*	R	6,507,118	01/03	Schueller			

U.S. Published Patent Documents

Examiner Initial	No.	Publication No.	Date	Name	Class	Sub-class	Filing Date
*	S	20030087475	5/2003	Sterrett et al.			
*	T	20020171152	11/2002	Miyazaki			
*	U	20020109228	8/2002	Buchwalter et al.			
*	V	20030001283	1/2003	Kumamoto			

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
*	W	Kulicke & Soffa, "Flip Chip Products, Polymer Collar Wafer Level Package; Achieve Maximum Reliability for Wafer Level Packages!", December 7, 2001, www.kns.com
*	X	Kulicke & Soffa, "Flip Chip Division, Polymer Collar Wafer Level Package; See the Polymer Collar WLP difference!", December 7, 2001, www.kns.com
*	Y	"Fundamentals of Microsystem Packaging", Rao R. Tummala, Chapters 2, 10, and 17, (May 8, 2001) McGraw-Hill Professional Publishing; ISBN: 0071371699
*	Z	"Chip Scale Package: Design, Materials, Process, Reliability, and Applications", John H. Lau and S.W. Ricky Lee, Chapter 1, Pages 1-41, (February 28, 1999) McGraw-Hill Professional Publishing; ISBN: 0070383049.
	AA	"All Dressesd Up and Nowhere to Go", Bogatin, Eric, Contributing Editor, May 1, 2002, Semiconductor, Downloaded on 12/23/2003 from http://www.reed-electronics.com/semiconductor/index.asp?layout=article&articleid=CA213812&rid=0&rme=0&cfd=1, 2 pages
	BB	Kulicke & Soffa, "Polymer Collar WLP™, Wafer Level Package Family" ©2002, 2 pages. http://www.kns.com/prodserv/PDFS/FCD/polymer_collar.pdf
	CC	"Polymer Collar WLP™ - A New Wafer Level Package for Improved Solder Joint Reliability", Barrett et al., Kulicke & Soffa - Flip Chip Division, Downloaded from: http://www.kns.com/resources/articles/PolymerCollar.pdf, 9 Pages
	DD	Kulicke & Soffa, "Presenting Polymer Collar WLP™ - A New Wafer Level Package for Improved Solder Joint Reliability", © 2002, Downloaded from: http://www.kns.com/prodserv/flipchip/pdf/PC_ad.pdf , 1 page.

Examiner	Date Considered

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